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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/072,684	02/07/2002	William John Devey	BEA920010039US1	2510

7590 07/03/2003

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EXAMINER	
VIGUSHIN, JOHN B	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 07/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/072,684	DEVEY, WILLIAM JOHN	
	Examiner	Art Unit	
	John B. Vigushin	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 February 2002* .

2a)☐ This action is **FINAL.** 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,6-9,11,13-21,23 and 25-31* is/are rejected.

7)☒ Claim(s) *3,5,10,12,22 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *0202* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 15-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 15 recites the limitation "said conductive plates of said I/C chip structure" in lines 9-10. There is insufficient antecedent basis for this limitation in the claim. The conductive plates belong to the capacitor; not to the IC chip. The rejection may be overcome by replacing "conductive plates of" with --active devices on-- in line 10.

Claims 16-19 depend from Claim 15 and therefore inherit the defect of the claim.

Rejections Based On Prior Art

3. The following references were relied upon for the rejections hereinbelow:

Li (US 2002/0195700 A1)* Mosley (US 2002/0071258 A1)

Li et al. (US 6,559,484 B1)**

*Hereinafter referred to as Li (A1).

**Hereinafter referred to as Li et al. (B1)

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 2, 4, 6-9, 11-14, 20, 21 and 23-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Mosley in view of Li (A1).

As to Claim 1:

I. Mosley discloses, in Figs. 1A and 5, and p.3: [0025]: PCB 506 having first and second opposite faces and vias 510 extending from each of the faces; an IC chip structure 515 with at least one active device thereon (typically, a die such as die 303 of Fig. 3; p.2: lines 3-6 of [0023]); connectors 512 connecting the active devices of IC chip structure 515 to vias 510 on one face of PCB 506; decoupling capacitor 503 (Fig. 1A) comprising: at least two interlaced conductive plates (plates 103 and 104 interlaced with plates 105 and 106; pp.1-2: lines 3-6 of [0018]) in dielectric material 113 (pp.1-2: line 16 of [0018]) forming at least one capacitor 100 (in Fig. 1A) or 503 (in Fig. 5); vias 115-118 extending from each of plates 103-106 through dielectric material 113to connect each via 115-118 to a circuit boar via 510 on the second face of PCB 506; vias 115-118 in decoupling capacitor (100 in Fig. 1A or 503 in Fig. 5) being parallel to each other (Fig.

1A) and each via 115-118 connected to one of conductive plates 103-106 being located adjacent a via 115-118 connected to another of conductive plates 103-106 (Fig. 1A).

II. Mosley discloses, in the embodiment of Fig. 2, at least two voltage planes 221 and 224 in PCB 206 and vias extending from a face of PCB 206 to the voltage planes 221 and 224 to which the capacitor 100 is connected but does not show such voltage planes in the embodiment of Fig. 5.

III. Li (A1) discloses, in Fig. 5, capacitors 506 mounted to a PCB 502 having and IC chip 508 mounted thereon, first and second opposite faces and vias extending from each of the faces to one of at least two voltage planes 512 and 514 which function as power or ground planes for the operation of capacitor 503 and IC chip 508.

IV. Since Mosley and Li (A1) are in the same art of fabricating electronic packages with decoupling capacitors, extending the vias of Mosley to power/ground voltage planes to operate the IC chip and capacitor, as taught by Li (A1) would have been readily recognized in the pertinent art of Mosley, and therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide at least two power/ground voltage planes in the PCB of Mosley and to extend each of the vias of Mosley to one of the power/ground voltage planes in order to operate the IC chip and decoupling capacitor, as taught by Li (A1).

As to Claims 2, 9 and 21, modified Mosley discloses that vias 510 in PCB 506 are arranged in the same pattern as vias 115-118 in capacitor 503 (Figs. 1A and 5; also see Figs. 1A,B in conjunction Fig. 2 and with pp.1-2: last six lines of [0018] and Fig. 2, wherein the relationship between vias 115-118 in capacitor 100 and voltage planes and

vias 221 and 224 in substrate 206 is the same as in the embodiment of Fig. 5, as modified by Li).

As to Claims 4, 11 and 23, modified Mosley discloses that vias 510 of PCB 506 and vias 115-118 of capacitor 100 (503) are each arranged in a straight line (see the capacitor vias in Fig. 1A of Mosley and the vias of PCB 506 as modified by Li (A1) in Fig. 5 of Li (A1)).

As to Claims 12 and 24, modified Mosley discloses that vias 510 of PCB 506 and vias 115-118 of capacitor 100 (503) and the vias in IC chip structure are each arranged in a straight line (see the capacitor vias in Fig. 1A of Mosley, IC chip 206 vias in Fig. 2 and p.2: lines 3-6 of [0022] and the vias of PCB 506 as modified by Li (A1) in Fig. 5 of Li (A1)).

As to Claims 6, 13 and 25, modified Mosley discloses that each via 115-118 in decoupling capacitor 100 (503) connected to one via of circuit board 506 (as modified by Li) is completely surrounded by vias in decoupling capacitor 100 connected to another of conductive plates 103-106 (Figs. 1A,B).

As to Claims 7, 14 and 26:

I. Modified Mosley does not disclose solder balls provided to decoupling capacitor 503 in Fig. 5 to connect the capacitor to PCB 506 but does evidently teach that pads 133 are used as the interconnection means between capacitor 503 and corresponding chip-receiving pads no PCB 506. However, Mosley further teaches that pads 133 can be used as the above-mentioned interconnection means sites or as a cite for C4 solder balls which also function as an interconnection means; i.e., capacitor 503

can be connected to PCB 506 using C4 solder balls on pads 133 or directly by means of pads 133 (pp.1-2: the last 8 lines of [0018]).

II. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to interconnect capacitor 503 to PCB 506 using the C4 solder balls, as taught by Mosley in the embodiment of Fig 2, since Mosley indicates that the use of C4 solder balls on pad sites 133 and pads 133 are art-recognized equivalent interconnection means which are selected according to the requirements of a particular application.

As to Claims 8 and 20:

I. Mosley discloses, in Figs. 1A and 5, and p.3: [0025]: PCB 506 having first and second opposite faces and vias 510 extending from each of the faces; an IC chip structure 515 with at least one active device thereon (typically, a die such as die 303 of Fig. 3; p.2: lines 3-6 of [0023]); connectors 512 connecting the active devices of IC chip structure 515 to vias 510 on one face of PCB 506; a discrete decoupling capacitor 503 (Fig. 1A) comprising: at least two interlaced conductive plates (plates 103 and 104 interlaced with plates 105 and 106; pp.1-2: lines 3-6 of [0018]) in dielectric material 113 (pp.1-2: line 16 of [0018]) forming at least one capacitor 100 (in Fig. 1A) or 503 (in Fig. 5) connected to the other face of PCB 506; vias 115-118 extending from each of plates 103-106 through dielectric material 113to connect each via 115-118 to a circuit boar via 510 on the second face of PCB 506; vias 115-118 in decoupling capacitor (100 in Fig. 1A or 503 in Fig. 5) being parallel to each other (Fig. 1A) and each via 115-118

connected to one of conductive plates 103-106 being located adjacent a via 115-118 connected to another of conductive plates 103-106 (Fig. 1A).

II. Mosley discloses, in the embodiment of Fig. 2, at least two voltage planes 221 and 224 in PCB 206 and vias extending from a face of PCB 206 to the voltage planes 221 and 224 to which the capacitor 100 is connected but does not show such voltage planes in the embodiment of Fig. 5.

III. Li (A1) discloses, in Fig. 5, capacitors 506 mounted to a PCB 502 having and IC chip 508 mounted thereon, first and second opposite faces and vias extending from each of the faces to one of at least two voltage planes 512 and 514 which function as power or ground planes for the operation of capacitor 503 and IC chip 508.

IV. Since Mosley and Li (A1) are in the same art of fabricating electronic packages with decoupling capacitors, extending the vias of Mosley to power/ground voltage planes to operate the IC chip and capacitor, as taught by Li (A1) would have been readily recognized in the pertinent art of Mosley, and therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide at least two power/ground voltage planes in the PCB of Mosley and to extend each of the vias of Mosley to one of the power/ground voltage planes in order to operate the IC chip and decoupling capacitor, as taught by Li (A1).

6. Claims 15-19 and 27-31 are rejected under 35 U.S.C. 102(e) as being anticipated by Li et al. (B1) in view of Li (A1) and Mosley.

As to Claims 15 and 27:

I. Li et al. (B1) discloses, in Fig. 6: a PCB 630 having first and second opposite faces; an IC chip structure 620 having first and second faces and at least one active device thereon, connectors 625 connecting active devices on IC chip structure 620 through the first face of IC chip structure 620 to PCB 630; a discrete decoupling capacitor 610 connected to IC chip structure 620 through second face of IC chip structure 620.

II. Li et al. (B1) does not disclose: 1) vias and voltage planes in PCB 630, wherein the vias extend from a PCB face to one of the voltage planes and the IC chip connectors 625 connect the active devices to the PCB vias on one face of the PCB 630; 2) a discrete decoupling capacitor structure comprising at least two interlaced conductive planes in dielectric material forming at least one capacitor connected to the active devices on IC chip structure 620; 3) vias extending from each of the conductive plates through the dielectric material to connect each via to a connector on the second face of IC chip structure 620; 4) the vias in decoupling capacitor 610 configured and arranged such that the vias are parallel to each other, and each via connected to one conductive plate is located adjacent a via connected to another conductive plate.

III. Li (A1) discloses, in Fig. 5, vias 510 and power/ground voltage planes 512, 514 in PCB 502, wherein the vias extend from a PCB face to one of the voltage planes 512, 514 and the connectors (balls) of IC chip 508 connect the active devices to the PCB vias 510, thus enabling operational power/ground connections to chip 508.

IV. Mosley discloses, in Figs. 1A and 2: a discrete decoupling capacitor 100 in Fig. 5) structure comprising at least two interlaced conductive plates 103-106 in

dielectric material 113 forming at least one capacitor connected to the active devices on IC chip structure 206 (Fig. 2; p.2: lines 3-6); vias 115-118 extending from each of the conductive plates 103-106 through the dielectric material 113 to connect each via 115-118 to a connector 218 on the second face of IC chip structure 206 (Fig. 2); 4) the vias in decoupling capacitor 100 configured and arranged such that the vias 115-118 are parallel to each other, and each via 115-118 connected to one conductive plate 103-106 is located adjacent a via 115-118 connected to another conductive plate 103-106 (Fig. 1A).

V. Since Li et al. (B1) is in the same art of mounting decoupling capacitors to electronic packages as Li (A1) and Mosley, and both Li (A1) and Mosley having similarly structured packages and components thereon, then the power planes and via structure in the PCB of Li (A1), including the connections of the PCB to the IC chip mounted thereon, and the via and interlaced conductive plate structure of the decoupling capacitor in Mosley, including the connections of the capacitor to the chip, would have been readily recognized in the pertinent art of Li et al. (B1) in order to establish the interconnections between capacitor, IC chip structure and PCB, thereby providing signal and power connections for package operation, as taught by Li (A1) and Mosley.

VI. Therefore, it would have obvious to one of ordinary skill in the art at the time the invention was made to include the above-cited structures of Li (A1) and Mosley in the PCB, IC chip and decoupling capacitor of Li et al. (B1) in order to establish the required operational connections between the PCB, IC chip and decoupling capacitor in the package of Li et al. (B1), as taught by Li (A1) and Mosley.

As to Claims 16 and 28, Li et al. (B1) in Fig. 6, as modified by Li (A1) and Mosley, discloses that the IC chip structure 610 (see IC chip 206 in Mosley) has vias therein arranged in the same pattern as that of the vias of capacitor 610 (see vias 115-118 of capacitor 100 in Mosley: Figs. 1A and 2), and each of the vias arranged in the IC chip structure being connected to the active devices (recall the element 206 is disclosed by Mosley as either a PCB or a die; p.2: lines 3-6 of [0022]).

As to Claims 17 and 29, Li et al. (B1) in Fig. 6, as modified by Li (A1) and Mosley, discloses that vias in decoupling capacitor 610 (see vias 115-118 in decoupling capacitor 100 of Mosley in Fig. 1A) and the vias in the IC chip structure 620 (see the vias in the IC chip structure 206 of Mosley in Fig. 2) are each arranged in a straight line.

As to Claims 18 and 30, Li et al. (B1) in Fig. 6, as modified by Li (A1) and Mosley, discloses that each via in decoupling capacitor 610 connected to one via in PCB 630 is completely surrounded by vias in the capacitor 610 connected to another conductive plate (see vias 115-118 and conductive plates 103-106 of Mosley in Fig. 1A).

As to Claims 19 and 31, Li et al. (B1) discloses, in Fig. 6, that solder balls 615 are provided connecting decoupling capacitor 610 to IC chip structure 620.

Allowable Subject Matter

7. Claims 3, 5, 10, 12, 22 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter:

As to Claims 3 and 5, 10 and 12, and 22 and 24, patentability resides in the limitation wherein the IC chip structure has vias therein arranged in the same pattern as the pattern of the vias in the decoupling capacitor, in combination with the other limitations of the broadest claims, Claims 3, 10 and 22, respectively.

9. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Yoon (US 6,320,249 B1) discloses a PCB 120 having a top surface and a bottom surface, an IC chip 170 mounted on the top surface of PCB 120 and a multilayer filter 110 having vias 116 and connected to the bottom surface of PCB 120 (Fig. 2), the multilayer filter 110 comprising a capacitor 111, inductor 119 and resistor 117 (Fig. 3).

b) Hernandez et al. (US 4,734,818) discloses a multilayer capacitor 80 with vias 90′ (Figs. 11-13) and an exemplary package with capacitor 216′ mounted on the bottom surface of PCB 212′ and IC chip 210′ mounted on the top surface (Figs. 2C, 2D).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 703-308-1205. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on 703-305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7382 for regular communications and 703-308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

John B. Vigushin
Examiner
Art Unit 2827

jbv
June 27, 2003